Chip Scale Package Joint Integrity Under Isothermal Aging

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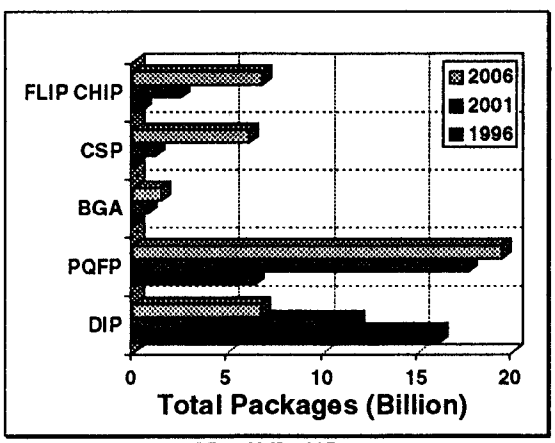
ABSTRACT

The popularity of emerging miniaturized Chip Scale Packages (CSPs) is rapidly growing because of their benefits and smaller size, though they may be considered to be an interim solution. There are more than forty CSPs available from different sources with only a few applications. Implementation will be facilitated as the necessary infrastructure is developed. Many aspects of this technology, with focus on assembly reliability characteristics, are being investigated by the JPL-led MicrotypeBGA consortium. Three types of test vehicles were considered for evaluation and currently two configurations have been built to optimize attachment processes. These test vehicles use numerous package types. To understand potential failure mechanisms of the packages, particularly solder ball attachment, the grid type packages were subjected to environmental exposure. Package I/Os ranged from 40 to nearly 300. The CSP packages were subjected to visual inspection and scanning electron microscopy (SEM) to characterize their joint quality, solder ball metallurgy, and elemental compositions. They were then subjected to ball shear testing, with results compared to the plastic ball grid arrays. After initial testing, these CSPs along with BGAs were subjected to isothermal aging at two different temperatures for two intervals. The exposed packages were then subjected to inspection, SEM, and shear testing, and the levels of damages documented. This paper presents the CSP test results.

MINIATURIZATION TRENDS

Projection regarding the use of through hole and surface mount IC packages are significantly differ and the numbers depend on the marketing source. One projection from the BPA, UK, is shown in Figure 1. Several trends are apparent.



Source: Adapted from BPA, SMI, 1997

Figure 1 Projection for Package Use (1996-2006)

The Dual In Line Package (DIP) had the most reduction in use, decreasing from 16 billion in 1996 to about 5 billion in ten years, i.e., about a one billion reduction per year. In contrast, the use of surface mountable packages including PQFPs (Plastic Quad Flat Packs) projected to increase in the next decade. The increase forecasted from 7 to 18 billion within the first five years and will almost plateau with an increase of only two billion for another five years. Within ten years, the COB (Chip On Board), not shown in Figure, expected to increase from 5 billion to 13 billion.

The increase in the use of CSP and flip chip packages are the same, projected to reach 6 billion by 2006. In contrast, the increase in BGAs for the same ten years is expected to be minimal, reaching to total use of only 1.5 billion. The projection for BGAs indicates that perhaps these packages were only an interim solution and were the stepping stone for the industry's wider acceptance of flip chip and chip scale packages. CSPs meet better the demands for denser and lighter towards miniaturized applications.

Why Chip Scale Packages

Emerging CSPs are competing with bare die assemblies. Many manufacturers now refer to CSP as the package that is a miniaturized version of the previous generation. Two concepts of CSPs are shown in Figure 2. The concepts include: (1) packages with flex or rigid interposer and (2) wafer level molding and assembly redistribution.

Packaging accomplishes many purposes, including the following:

- Provides solder balls and leads that are compatible with the PWB pad metallurgy for reflow assembly processes.

- Redistributes the tight pitch of the die to the pitch level that is within the norm of PWB fabrication. The small sizes of CSPs do not permit significant redistribution and current cost effective PWB fabrication limits full adqption of the technology, especially for high I/O counts.
- Protects the die from physical and alpha radiation damages, and provides a vehicle for thermal dissipation.
- Eases die functionality testing.

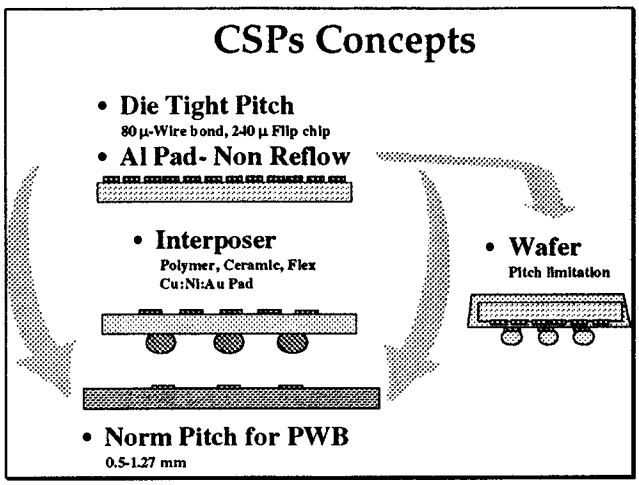


Figure 2: Two Chip Scale Package Concepts

Self Alignment of Grid BGAs

CSPs can be categorized into grid arrays and leads or no leads using I/O expandability and manufacturing robustness as shown in Figure 3. Key advantages/disadvantages of each category are also listed.

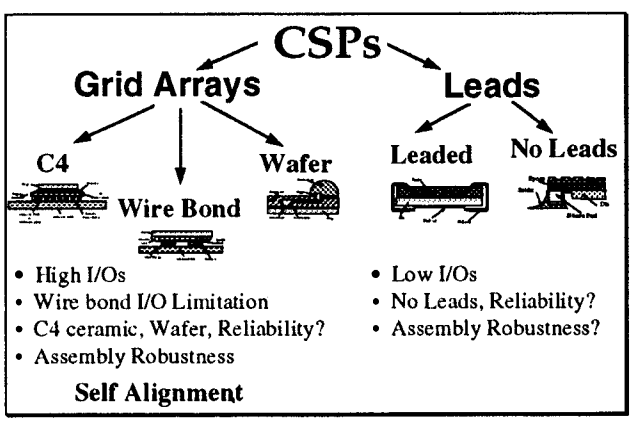


Figure 3: Two Chip Scale Package Categories

The mini (fine pitch) grid arrays can accommodate higher pin counts, and similarly to BGAs, they have self alignment (centering) characteristics. For BGAs, the ease of package placement requirements has been widely published as one of their advantages. This attribute has permitted reduction in the number of solder joint defects to lower levels than conventional SM packages.

Many factors affect self alignment characteristics, but the main factor is the molten solder surface tension that provides the pull force on the package toward the pad centers. The counter force is the weight of the package. For Plastic BGAs (PBGAs), the pull forces induced from the melt of eutectic balls are larger than the forces from the partial molten joints in the ceramic BGAs (CBGAs) or solder paste melts in conventional packages. Hence, better self alignment for PBGAs. The symmetry of BGA ball patterns helps further in permitting both X and Y as well as rotational placement offsets for BGAs.

For grid CSPs, the molten surface tensions are much smaller than BGAs since they have lower solder ball volumes. This, coupled with the CSPs finer pitch, can derate their self alignment performance, especially with heavy packages. Therefore, the CSPs might require much tighter placement accuracy than the 50 mil pitch BGAs.

Grid CSPs show self alignment, but there is disagreement on best offset limits.

- An offset of only 25% for a grid CSP with 46 I/Os was found to be acceptable. The acceptable offsets were 62% for PBGAs and 50% for CBGAs (Noreika, Surface Mount International (SMI), 1997).
- An offset of 80% reported by another investigator (Patridge, SMI '97).
- Only two bridges out of 16,100 solder joints were reported. These were due to foreign materials with no defects found due to placement inaccuracy. The test was a qualitative determination in which three hundred CSPs with 46 I/Os were hand placed, reflowed, and joint defects were then characterized (Bauer, et al, SMI '97).
- Only two solder joint shorts were detected out of 200 hundred assembled CSP packages with 44 I/Os (Hunter, et al, CHIPCON '98).

Thermo-mechanical Failures

The thermo-mechanical wear (creep) of solder joints is the cause of failure for most CSP board assemblies. Failure at the board level can also be due to package internal failure or from the solder balls/package interface in grid CSPs.

A non-uniform thermal expansion and/or contraction of different materials in the assembly induces

mechanical stress on solder joints. To achieve the least damage to solder joints, thermal mismatch between the die and board should be minimized either by package optimization or use of board materials that closely match coefficient of thermal expansion (CTE) of the package.

Only a few CSP packages have been designed to alleviate damage due to the thermal expansion of package/board mismatches. The floating pad technology (FPT) is another technique that was recently conceived with the aim of absorbing CTE mismatches at the pad level (Wojnarowski, ITAP '98). The literature data on assembly reliability of a CTE absorbed package along with numerous other packages were presented previously[1,2].

Failure Shift

Assembly failure can be misinterpreted when there is a shift in failure mechanisms. For example, package internal TAB lead failures at heels were reported for the CTE absorbed CSP— a fatigue failure mechanism shift from the solder joint to the internal package. An example of cycles to failure theoretical projection with no consideration on failure shift is shown in Figure 4. A life of more than 7,000 cycles for a thermal cycle profile of -55°C to 125°C was projected. This is an order of magnitude larger than experimental cycles to failure of 1,000 to 1,500 cycles. The TAB failure just before assembly failure was detected at 1,000 cycles (Greathouse, CHIPCON '96)

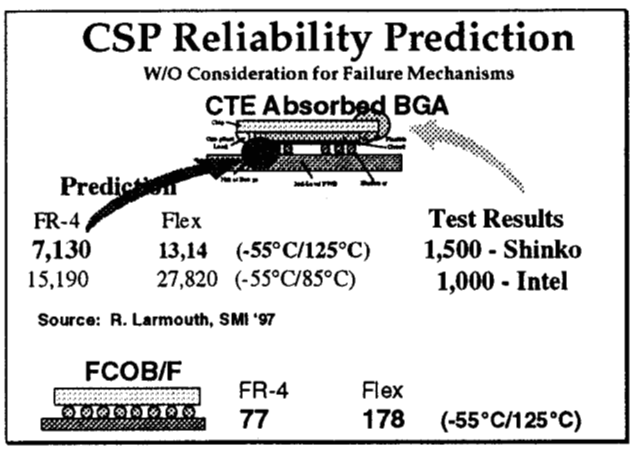


Figure 4 Fatigue Failure Projection based on the Wrong Failure Mechanism Assumption for a CTE Absorbed CSP

Ball/Package Interface Failure

For grid CSPs, the interface between package and solder balls is another potential failure site. This failure type was observed for plastic BGAs after thermal cycling. For BGAs, cycles to failure and failure mechanisms under different environments were investigation under another program. Figure 5, adapted from Reference 3, shows cumulative failure percentages versus increasing cycles for several plastic BGA assemblies. Wider distribution for two peripheral BGA packages are evidenced from this figure.

The exact causes of wider distributions are yet to be identified. Possible causes include: PWB materials (FR-4, polyimide), solder volume, and ball/package integrity. Package/ball integrity plays a role since failure analyses of cycled BGA assemblies indicated that failures occurred either at package or board interfaces. This means that solder joint cycling test results for packages from prototype or early production might not be representatives of full production results. Wider distributions are also expected if processes are not optimized.

This investigation included BGAs as well as grid CSPs to determine if there were differences in package/ball interface integrity before and after isothermal exposure and if this correlated with cycles to failure test results. The isothermal temperatures were the maximum thermal cycling temperatures. The grid CSPs were from the list of leaded, leadless, and CSPs. Their board assemblies are being evaluated by the JPL-led MicrotypeBGA consortium.

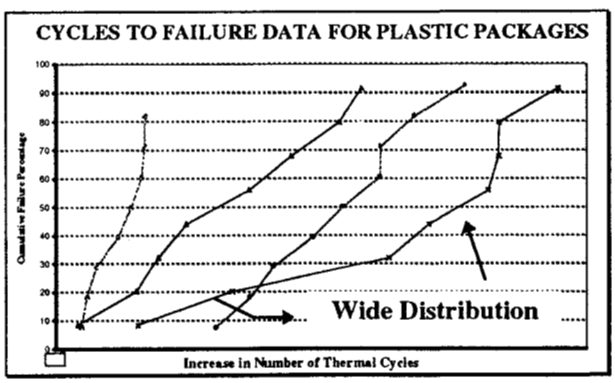


Figure 5 Wide Distribution for Two BGA Package Types

SEM Characterization

Representative SEM photomicrographs of CSP ball shapes and their interfaces are shown in Figure 6. Photos for a TAB CSP from two suppliers are shown in a and b, and for a wafer version in c. Note differences in interfaces for the same package, but from two suppliers as well as different package categories. The TAB CSP-1 had a non solder mask defined configuration whereas the CSP-2 had a solder mask defined appearance. These differences might not be significant for this specific package since this CSP is a

CTE absorbed package and assembled failure is not expected to be from the solder joint.

Shear Forces Before Isothermal Exposure

Figure 7 shows cumulative percentage versus shear forces for various packages. The median ranking (i-0.3/n+0.4) was used to calculate cumulative percentages. The fifty percentile shear forces as well as their respective shear stresses are shown in Table 1. It is interesting to note the significant difference in shear forces for different packages. Distributions for the same packages, but different suppliers are different. CSP-2 with a solder mask defined configuration has a tighter force distribution.

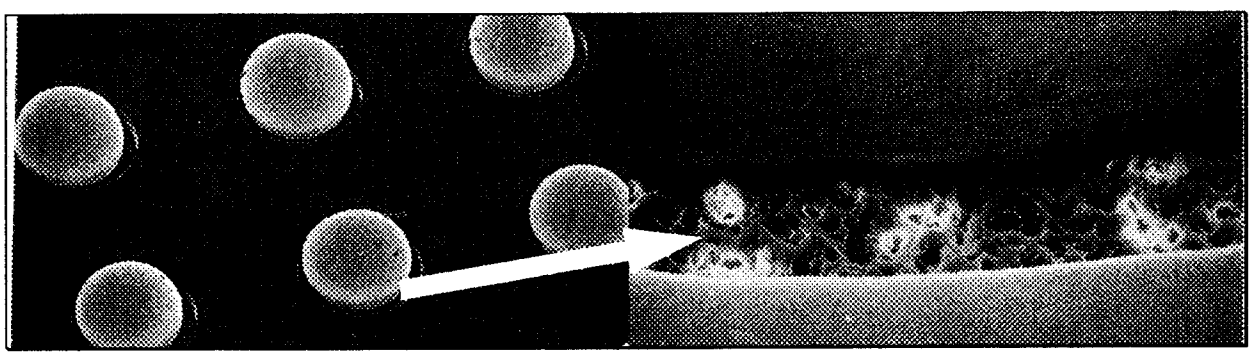
SEM of Shear Failures

SEM photomicrographs for three CSPs are shown in Figure 8. Generally failures were ductile and were from the balls to package pad interfaces. Two of the balls from the CSP-1 failed in the traces (see right photo of (a)). The non-uniformity in interface failures for CSP-1 might be the reason for this package's wider force distribution plots in Figure 7.

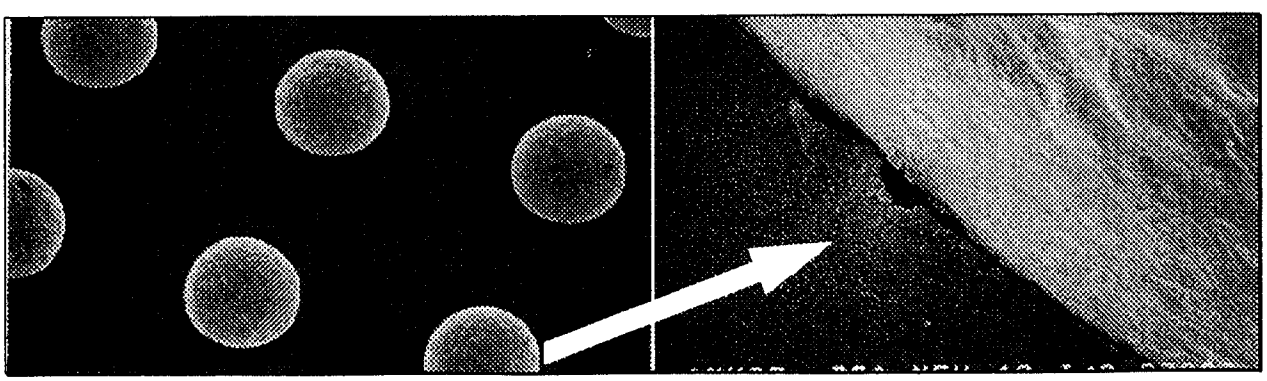
Shear Forces after Isothermal Exposure

Results for those exposed to 100 hours at 100°C are also shown in Figure 7. The wafer level package showed improvement after exposure. The most probable cause of this improvement is microstructural changes which could have reduced the processing residual stresses. This was not verified.

(a) Wafer Level CSP



(b) TABCSP-1



(c) TABCSP-2

Figure 7 Ball/Package Configurations for Various CSPs

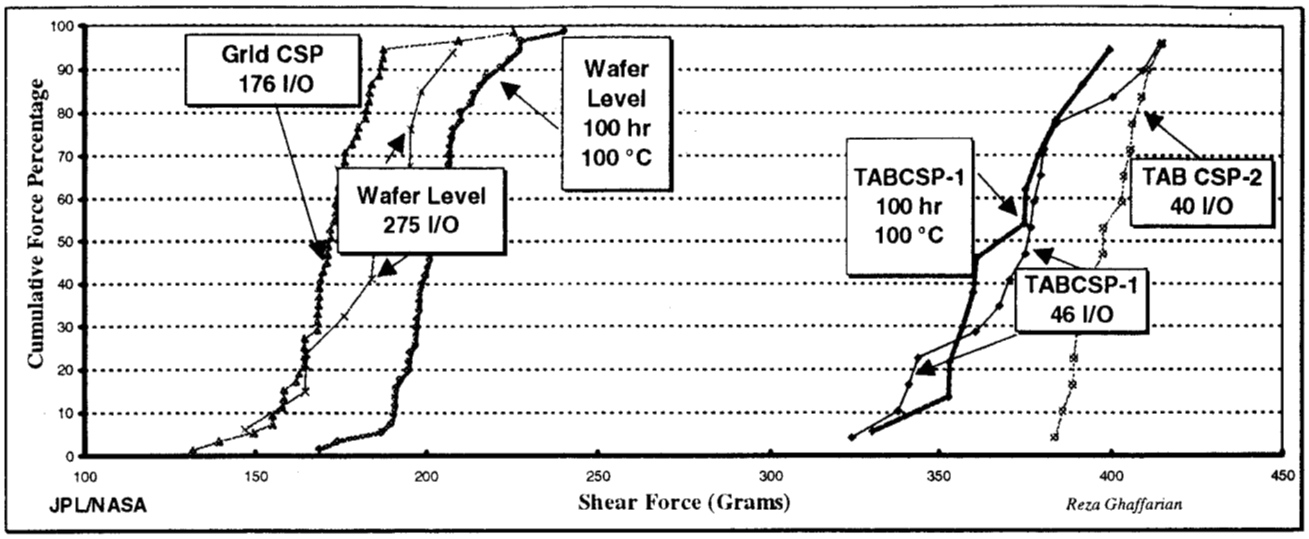
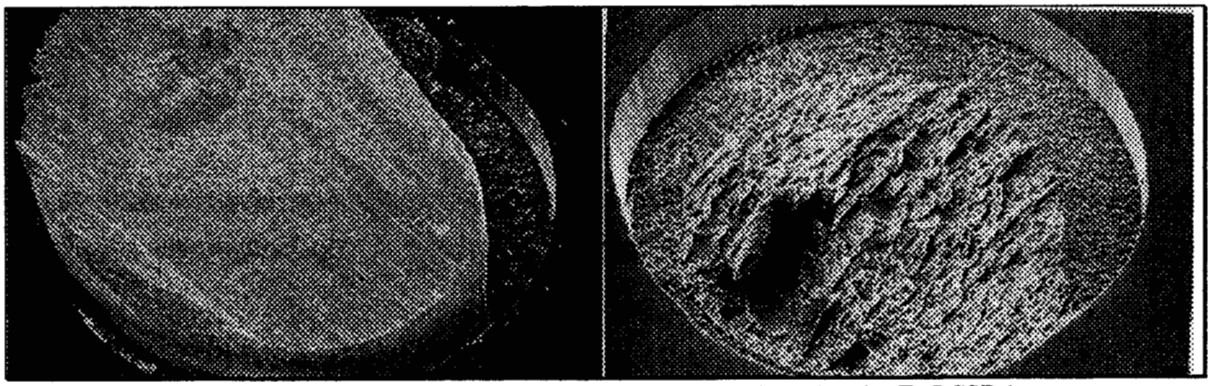


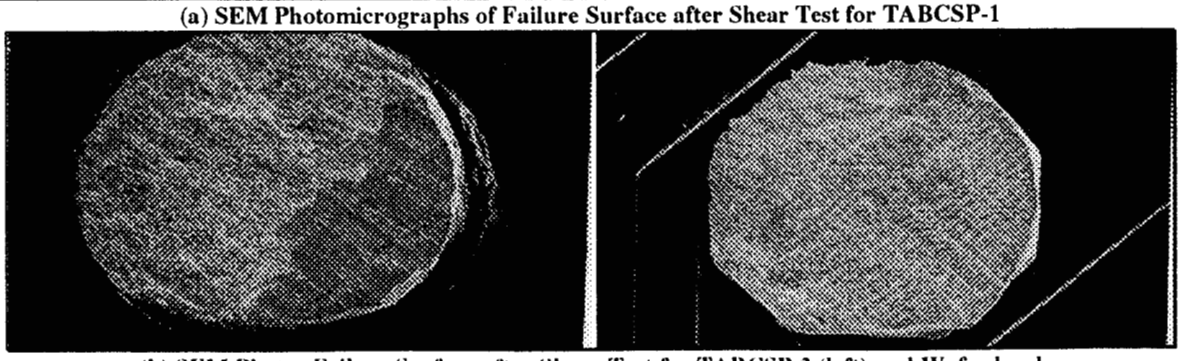
Figure 7 Shear Force Distribution for Various CSPs

Table 1 Shear force and stress for various CSPs

Package Type	I/O	Shear Diameter (mm)	Shear Force (grm) at 50%	Shear Stress (grm/mm^2)	Shear Stress 100 Hours at 100°C
TABCSP-1	46	0.320	376	4,676	4,663
TABCSP-2	40	0.30	397	5,616	N/A
Wafer CSP	275	0.250	185	3,768	4,094
GridCSP	176	0.170	172	7,576	N/A



(a) SEM Photomicrographs of Failure Surface after Shear Test for TABCSP-1



(b) SEM Photos Failure Surface after Shear Test for TABCSP-2 (left) and Wafer level

Figure 9 SEM Photos of Failure Surface after Shear Tests for Various CSPs

CONCLUSIONS

- The allowable offset placement levels which result in grid CSP acceptable assembly are not well established. It was postulated that a tighter placement control might be required for CSPs, than BGAs.
- Failure shift from solder joint to package may occur more often for miniaturized CSP packages. Projection based on the wrong failure mode results in wrong forecast cycles for failure.
- The MicrotypeBGA consortium was formed to systematically address many of the CSP assembly reliability issues. The ball/package characterization performed was aimed at understanding of other-than-board solder joint sources of assembly failures.
- Ball shear forces were differ for different CSPs. Shear force distributions for the same package type differ for two suppliers.
- Difference in shear forces depended on many variables including interface area, metallurgy, solder mask defined or non defined, and failure mechanisms.
- Slight improvement in shear force or narrower distribution was observed after packages exposure at 100°C for 100 hr. Improvement may be due to stress relaxation by annealing.
- Assembly handling could be an issue for those CSP packages with low resistance to shear force. Lower value in force did not translate to lower shear strengths (force/area).

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ACKNOWLEDGMENTS

The research described in this publication is being carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

I would like to acknowledge in-kind contribution and cooperative efforts of the MicrotypeBGA consortium team members and those who have been contributing to the progress of the program. Especial thanks to J. Okuno and K. Evans for performing shear tests and SEM characterizations.